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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/429,094	10/28/99	YATES J	30585/16

TM02/0410

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EXAMINER	
ENG, D	
ART UNIT	PAPER NUMBER
2155	8

DATE MAILED: 04/10/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/429,094	Yates et al.
Examiner	**Group Art Unit**
David Y. Eng	2155

☒ Responsive to communication(s) filed on *Oct 16, 2000*

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *three* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) *1-35* is/are pending in the applicat

Of the above, claim(s) _____ is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-35* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☐ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). *5*

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

— SEE OFFICE ACTION ON THE FOLLOWING PAGES —

Claims 24-35 have been added. The active claims are 1-35.

The amendment at page 62, lines14-15, replacing "the operating system" with --Tapestry operating system 312-- has not been entered because the text is not at the location.

The Examiner is unable to find what TAXi stands for or what it represents in the specification.

Claims 1-35 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 is rejected as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP 2172.01. The omitted element is a table which stores the entries accessed and used by the table lookup circuitry and by the handler respectively. Other claims have similar defect.

Claim 1 fails to recit what event causes the interrupt. Note that instruction addresses and memory state are not events. Although the claim recites that entries are accesed for use at each basic instruction cycle, the claim fails to recite at which point of time the interrupt handler is triggered to use the entry to make the decision. Other claims have similar defect. See claims 9, 12, 18, 19 and 29 for example.

Further with respect to calim 1, it appears that the handler is unable to make a decision as to whether to effect control of an architecturally-visible data manipultaion behavor or of a control transfer behavior of an instruction based on an entry describing a likelihood of the existence of an

alternate coding of the instruction. There is no apparant relationship between likelihood of existence and different behaviors. Other claims have similar defect. See claims 7, 14 and 24 for example.

Claim 8 fails to recite further method steps in regard to the memory structure recited therein. For example, steps for translating addresses, steps for accessing page and steps for accessing entries within the page, etc. Note that its parent claim is a method claim and not an apparatus one. Other claims have similar defect. See claim 27.

Scope of limitation of the following claim language is not clear:

1. "the architectural definition of the instruction not calling for an interrupt" in line 12 of claim 1. Applicants are requested to identify the definition in the specification. Other claims have similar defect. See claims 19 and 29 for example.

2. "an architecturally-visible data manipulation behavior or control transfer behavior of an instruction" in line 16 of claim 1. Applicants are requested to identify the definition in the specification. Other claims have similar defect.

3. "non-supervisor mode program" in line 10 of claim 1. Applicants are requested to identify the definition in the specification. Other claims have similar defect.

4. "different instruiction" in claim 3. It is not clear which instruction is a different instruction.

In claim 2, there is no clear antecedent basis for "the content of a table entry" in line 6.

In claim 5, it appears that the control of behavior per se is not related to changing of ISA.

The last paragraph of claim 10 is not understood. It is not clear what is being altered. It is not clear what is meant by "alter -- in a manner incompatible with the architectural definition of the instruction".

In claim 11, it is not clear at which point of time the table is accessed and the determination is ititiated. What triggers the table lookup and the initiation of determination?

In claims 13, 14, 20 and 28 there is no relationship recited between interrupt and change of behavior.

Claim 14 fails to recite functional relationship between the components. No meaningful or useful operation is seen from the claim.

Function of the interrupt handler as recited in claim 21 is not clear in that an interrupt handler which is commonly for handling interrupt is recited for changing ISA. It appears other structures, other than just the interrupt handler, are required.

Claim 22 is not understood. Scope of claim 22 is not clear. Further, it is not clear what is meant by "equivalent". The term is vague and indefinite. The two instruction text in the wherein clause of claim 22 have no clear antecedent basis.

Dependency of claim 26 is not clear.

Claims 30-35 have similar defects set forth above.

Applicants are requested to identify the following components in the drawings and the description thereof in the specification:

1. the table lookup circuitry,

2. the table with entry having the likelihood description

3. the interrupt circuitry and the handler,

4. the meaning of "the architectural definition of the instruction not calling for an interrupt", and

5. the description of the pipeline circuitry to effect control of an architecturally-visible data manipulation behavior and control transfer behavior.

Note that claim language should have support in the specification.

Claims 24 and 30 are rejected under 35 USC 112, 1st paragraph, as those claims are impermissible single means claims containing undue breath. (See MPEP 2164.08 (a) and 2181).

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1-13 and 19-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morley (5,751,982) in view of Woods (5,678,032).

See at least background of the invention, summary of the invention and the description of Figures 3 and 4 in Morley.

Morley teaches a microprocessor chip, comprising:

1. An instruction circuitry (CPU line 14, column 1),

2. A table lookup circuitry (dispatcher),

3. A table (16) having entries for indicating whether native code 18 or native code 26 should be accessed (therefore result in different behavior),

4. An interrupt circuitry (the emulator) cooperatively designed with the instruction circuirty to trigger an interrupt (when the emulator encounters an instruction or frequentlyy executed instruction to be emulated).

The only difference is that Morley did not specify that the instruction circuitry is a pipeline one. Instruction pipeline circuitry is well known in the art. Woods teaches an emulator having pipeline processor. Since both references are directed toward emulator and pipeline processor is well known in the art, it would have been obvious to a person of ordinary skill in the art to use a pipeline processor in Morley such that instruction execution can be pipelined.

Claims 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morley (5,751,982) , Woods (5,678,032) further in view of Bianchi (6,006,029).

Morley and woods disclose claim combination set forth above. Morley does not appear to have an address translator. However, Bianchi discloses an emulator having an address translator (item 5, column 18). Ti would have been obvious to a person of ordinary skill in the art to incorporated an address translator in Morley if address are required to be mapped or translated.

DAVID Y. ENG
PRIMARY EXAMINER